

THAT WHICH IS CLAIMED IS:

1. Non-volatile memory cell (10) of the type which comprises at least one floating gate transistor (12) realized, over a semiconductor substrate (13), with a source region (S1) and a drain region (D1) separated by a channel region (C1) which is overlaid by a thin layer (15) of gate oxide to isolate, from the substrate (13), a floating gate region (GF1) coupled to a control gate terminal (GC1), characterized in that said floating gate region (GF1) develops a first potential barrier (16) between the semiconductor substrate (13) and the gate oxide layer (15), while a second different potential barrier (17) is defined between the floating gate region (GF1) and the gate oxide layer (15).

2. A memory cell according to Claim 1, characterized in that said second potential barrier (17) is lower than said first potential barrier (16).

3. A memory cell according to Claim 1, characterized in that said floating gate region (GF1) comprises a first material having a lower electron affinity than the material of the semiconductor substrate (13).

4. A memory cell according to Claim 1, characterized in that said floating gate region (GF1) has a focused electric field.

5. A memory cell according to Claim 4, characterized in that said floating gate region (GF1) comprises a plurality of points (18) in the direction toward the gate oxide layer (15).

6. A memory cell according to Claim 5, characterized in that said plurality of points (18) are obtained using chemi-physical techniques of etching away the gate oxide layer (15).

7. A memory cell according to Claim 5, characterized in that said plurality of points (18) are obtained by nucleation of a further dielectric layer (19) deposited over the gate oxide layer (15).

8. A memory cell according to Claim 5, characterized in that said plurality of points (18) are obtained by introducing granules (20) of a conductive material into the gate oxide layer (15), in the
5 proximity of the floating gate region (GF1).

9. A memory cell according to Claim 1, characterized in that said floating gate region (GF1) comprises a first layer (5') of material of a first type adjacent to the surface of the semiconductor
5 substrate (13), and a second layer (21) of material of a second type whose electron affinity lies intermediate to those of said first material and the material of the floating gate region (GF1).

10. A method of making a low erase voltage, non-volatile memory cell (10) of the type which comprises at least one floating gate transistor (12) realized, over a semiconductor substrate (13), with a source
5 region (S1) and a drain region (D1) separated by a channel region (C1) which is overlaid by a thin layer (15) of gate oxide to isolate, from the substrate (13), a floating gate region (GF1) coupled to a control gate terminal (GC1), characterized in that a first potential
10 barrier (16) between the semiconductor substrate (13) and the gate oxide layer (15), and a second different

potential barrier (17) between the floating gate region (GF1) and the gate oxide layer (15), are provided.

11. A method according to Claim 10, characterized in that said second potential barrier (17) is lower than said first potential barrier (16).

12. A memory cell according to Claim 9, characterized in that said second layer (21) comprises silicon nitride.

13. A memory cell according to Claim 12, characterized in that the thickness of said second layer (21) is smaller than said first layer (5') thickness.

14. A memory cell according to Claim 13, characterized in that said second layer (21) is realized by deposition at a low temperature.

15. A memory cell according to Claim 3, characterized in that said first material has electron affinity in the range of 2.5eV to 3.5eV.

16. A memory cell according to Claim 3, characterized in that said first material is either a dielectric material or a metal.

17. A memory cell according to Claim 8, characterized in that said introduction of granules (20) is performed by low-energy implantation followed by a thermal treatment.

18. A memory cell according to Claim 8, characterized in that said introduction of granules (20) is performed by deposition of a thin layer of a

further material followed by an oxidation step and a step of isolating residual granules not fully oxidized.

19. A memory cell according to Claim 18, characterized in that said step of isolating residual granules not fully oxidized is performed by using, of preference, a grain-edge oxidation process.